Application No. 10/583,868
Reply to Office Action of September 15, 2008,
   and Advisory Action of December 18, 2008

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A data processor, comprising:

a CPU configured to control an entire system;

a DSP configured to perform preset processing, to have at least two bus cycles in a unit of one data access, and to use a selectable number of the bus cycles in the unit of one data access; and

an external memory configured to be accessed by the DSP and to be accessed through the DSP by the CPU, wherein

a data word length accessed by the DSP at the external memory is variable, and

the DSP includes

a determination unit configured to determine whether the DSP is accessing the external memory;

a control unit configured to determine whether the CPU is allowed to access the external memory, based on a signal from the determination unit; and

a switching unit configured to perform a switching operation of an address and a data in connection with the external memory according to a command from the control unit, and to input and to output the address and the data based on the switching operation,

wherein when the DSP accesses the external memory using a maximum number of the bus cycles in a unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is placed in a wait state until a subsequent unit of data access commences, and

when the DSP does not access the external memory using the maximum number of the bus cycles in said unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is constantly allowed during said unit

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of data access ~~data word length is selected so that the DSP accesses the external memory~~

~~using a maximum number of the bus cycles, when the determination unit determines that the~~

~~DSP is accessing the external memory, access from the CPU to the external memory is placed~~

~~in a wait state by the control unit, and when the data word length is not selected so that the~~

~~DSP accesses the external memory using the maximum number of the bus cycles, the control~~

~~unit is configured to allow the CPU to access the external memory by utilizing a free bus~~

~~cycle~~.

2. (Currently Amended) A data processor, comprising:

a CPU configured to control an entire system;

a sound source configured to supply a musical tone signal;

a DSP configured to perform preset processing to apply a desired effect to the musical

tone signal supplied from the sound source, to have at least two bus cycles in a unit of one

data access with respect to signal processing of the musical tone signal, and to use a

selectable number of bus cycles in the unit of one data access; and

an external memory configured to be accessed by the DSP and to be accessed through

the DSP by the CPU, wherein

a data word length accessed by the DSP at the external memory is variable, and

the DSP includes

a determination unit configured to determine whether the DSP is accessing the

external memory;

a control unit configured to determine whether the CPU is allowed to access

the external memory, based on a signal from the determination unit; and

a switching unit configured to perform a switching operation of an address and

a data in connection with the external memory according to a command from the control

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~~means~~ unit, and to input and to output the address and the data based on the switching

operation,

wherein when the <u>DSP accesses the external memory using a maximum number of</u>

<u>the bus cycles in a unit of data access wherein the DSP actually accesses the external</u>

<u>memory, access from the CPU to the external memory is placed in a wait state until a</u>

<u>subsequent unit of data access commences, and</u>

<u>when the DSP does not access the external memory using the maximum number of</u>

<u>the bus cycles in said unit of data access wherein the DSP actually accesses the external</u>

<u>memory, access from the CPU to the external memory is constantly allowed during said unit</u>

<u>of data access</u> ~~data word length is selected so that the DSP accesses the external memory~~

~~using a maximum number of the bus cycles, when the determination unit determines that the~~

~~DSP is accessing the external memory, access from the CPU to the external memory is placed~~

~~in a wait state by the control unit, and when the data word length is not selected so that the~~

~~DSP accesses the external memory using the maximum number of the bus cycles, the control~~

~~unit is configured to allow the CPU to access the external memory by utilizing a free bus~~

~~cycle~~.

3. (Currently Amended) A data processor having a fixed number of memory access

timings per sampling cycle, the data processor comprising:

a plurality of DSPs configured to access a single external memory in a single package;

~~an access determination unit configured to determine, when each of the DSPs issues a~~

~~read command or a write command at a same time, which one of the DSPs is allowed to~~

~~access the memory;~~

~~a read/write control unit configured to control, when each of the DSPs issues the read~~

~~command or the write command at the same time, a command of the allowed DSP;~~

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a read/write control unit configured so that when each of the DSPs issues a read

command or a write command at a same time, none of the commands from the DSPs are

performed and when only one of the DSPs issues the read command or the write command,

the command from the only one DSP is performed;

an access determination unit configured so that when each of the DSPs issues the read

command or the write command at the same time, none of the DSPs are not allowed to access

the external memory and when the only one of the DSPs issues the read command or the

write command, the only one DSP is allowed to access the external memory;

a first selector configured to output an address from the allowed DSP in response to a

determination signal from the access determination unit; and

a second selector configured to output data from the allowed DSP in response to the

determination signal, wherein

each of the DSPs includes a control unit configured to acquire data from the external

memory in response to the determination signal from the access determination unit, and

the read/write control unit does not access the external memory when each of the

DSPs simultaneously issues a command.

4. (Canceled).

5. (Currently Amended) A data processor having a fixed number of memory access

timings per sampling cycle, the data processor comprising:

a plurality of DSPs configured to access a single external memory in a single package,

the external memory storing musical tone waveform data;

an access determination unit configured to determine, when each of the DSPs issues a

read command or a write command at a same time, which one of the DSPs is allowed to

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~~access the memory; a read/write control unit configured to control, when each of the DSPs~~

~~issues the read command or the write command at the same time, the command of the~~

~~allowed DSP;~~

a read/write control unit configured so that when each of the DSPs issues a read

command or a write command at a same time, none of the commands from the DSPs are

performed and when only one of the DSPs issues the read command or the write command,

the command from the only one DSPs is performed;

an access determination unit configured so that when each of the DSPs issues the read

command or the write command at the same time, none of the DSPs are not allowed to access

the external memory and when only one of the DSPs issues the read command or the write

command, the only one DSP is allowed to access the external memory;

a first selector configured to output an address from the allowed DSP in response to a

determination signal from the access determination unit; and

a second selector configured to output data from the allowed DSP in response to the

determination signal, wherein

each of the DSPs includes a control unit configured to acquire data from the external

memory in response to the determination signal from the access determination unit, and

the read/write control unit does not access the external memory when each of the

DSPs simultaneously issues a command.

6. (Canceled).